International Journal of Computer Engineering and Information Technology

VOL. 11, NO. 4, April 2019, 59–64
Available online at: www.ijceit.org
E-ISSN 2412-8856 (Online)

A Comparative Study of Viterbi Decoding Algorithm for Code Rate (1/2) in AWGN Channel

Hiba.S. Mahmood[1] and Dr. Mohammed. H. Al-Jammas[2]

[1, 2] College of Electronics Engineering, Nineveh University, computer and information engineering

[1]hibasaad_1983@yahoo.com, [2]mohammed.aljammas@uoninevah.edu.iq

ABSTRACT

In this paper, a study on decoding the convolutional codes in AWGN channel using the Viterbi algorithm is presented. This study is performed using different constraint lengths at a fixed coding rate of (1/2). The performance of hard and soft Viterbi decoder is evaluated by measuring Bit Error Rate and decoding delays at various constraint lengths. Results show that Soft decoder provide around (1 to 2) dB of gain for bit error rate comparative of hard decoder. Increasing constraint length results in further improvement in BER in both soft and hard Viterbi decoders. Soft decoders, on the other hand, are shown to have less decoding time than hard decoders do. In digital communication systems, the use of hard or soft Viterbi decoder at a specific constraint length is a trade-off between decoding speed and accuracy of reconstructing original data.

Keywords: *Viterbi Decoder, Bit Error Rate, code rate, Constraint length.*

1. INTRODUCTION

In wireless communication systems, the interference and noise accrue and it is very high. It affects the Signal to Noise Ratio (SNR). Therefore, the Error Detection and Correction (EDC) techniques are needed to improve SNR [1]. Convolutional code is error correct techniques almost used in most of communication systems. Transmitter used convolution encoder add redundancy bits to the information before transmitted. Therefore, the effective technique to decode the convolutionally encoded data is Viterbi Decoder (VD). Viterbi decoder uses Viterbi algorithm to decode convolutionally encoded data. The decoder configuration depends on encoder's generator polynomial, code rate and constraint length. Decoder can be able to correct information bits corrupts by noisy channel through transition due to the structure of convolutional encoded code. The decoding will start from zero state by the assumption that the encoding will start from the same state. The Viterbi decoding select the low metric path to be winning path. The winning path will have low bit error path compared to other paths. Viterbi decoder implementation has two types namely hard decision and soft decision Viterbi decoding. In hard decision, a hamming distance metric is use, and in soft decision the Euclidean distance metric used. Hamming distance metric is the number of differ bits between received code and actual code and the path with lowest Hamming distance metric is called survivor path. If hamming distance is zero, this indicate that the symbol is receive without any error. Euclidean distance metric is squared difference between received symbol and actual symbol. The path with minimum Euclidean distance is called a survivor path. The received symbol in Soft decision decoding is quantized in to more than two levels, so the soft decision decoder is better than hard decision because soft decision decoding will have more information about the received information [2][3].

2. Convolutional Encoder

Convolution codes are one of the powerful and widely used in numerous applications because of ability of error correction [3]. The convolution encoding is done by entered a fixed number (m) of input data to encoder to result in an n_ bits symbol [4]. The input bits are passed through the shift register and merged using (XOR) gates with many outputs of shift register cells [5]. This process is equivalent to convolution method and is called a convolution coding [4]. A convolution encoder protects data by adding redundant bits into the binary data stream through the linear shift registers. Convolution encoder can be described by the three following parameters (n,m,L) as summarized:

n : number of output symbols.
m: number of input symbols.
L: number of shift register.

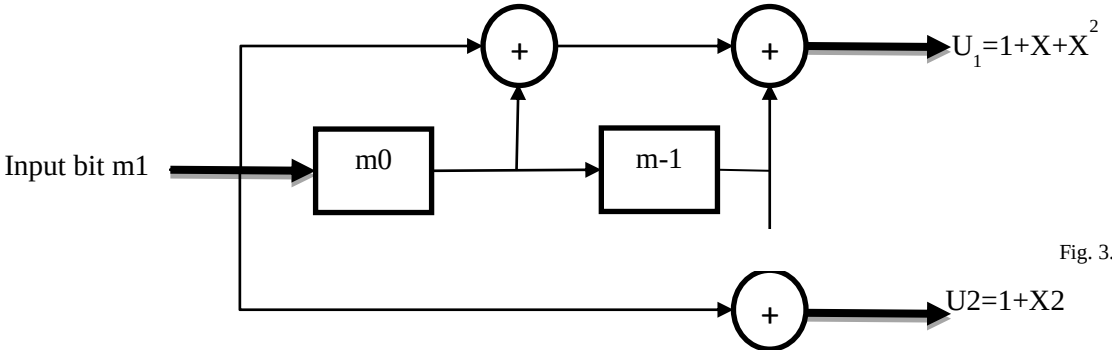


Fig. 1. Convolutional Coding with rate 1/2, Generator Polynomials 7, and 5

Constraint length (K) = L+1 is the number of stages which the input bit pass through in the encoding shift register [6]. Convolution encoder accepts an (m) input bits that are fed to the shift register and calculates (n) outputs from generator polynomials by (XOR). In generator polynomial, 1 refers to the connections and 0 indicates that there are no connections between shift register and (XOR) gates. Fig.1 shows a simple convolution encoder example with m=1, n=2, K=3, u1=111, u2=101 [7].

3. VITERBI DECODER

To decode a noisy signal received, the Viterbi decoder is used [8]. The Viterbi decoder is the most common way to decode convolutional code that may be corrupted through transmit [5]. The general flow of information over a noisy channel is shown in fig. 2.
The encoder adds to original information bits redundant bits for the purpose of error recovery. The output from encoder is transmitted across the channel. In the receiver, the data contains information with redundancy bits that may be corrupted through transmission, Viterbi decoder tries to extract the original information by start moving along the trellis in the front direction then make some calculations, after this in backward direction move to find the transmitted bits sequence before encoding [9]. Decoding complexity is the main drawback it growing exponentially with the length of code, so it can be used only for relatively short codes [8].

The computational complexity in Viterbi decoder can be reduced by using simpler trellis structure. Fig. 3 shows the general block diagram of Viterbi decoding algorithm, while fig.4 shows the flowchart of Viterbi decoder.
Viterbi decoder has three basic units [10]:

3.1 Branch Metric Unit (BMU)

The first unit in the Viterbi decoder is branch metric unit, this unit calculate the distance between received code from noisy channel and legal codewards. There are two measure in BMU, hamming distance in the case of hard input decoding or Euclidean distance when soft input decoding [5].

3.2 Add Compare Select Unit (ACSU)

The second unit is add compare select unit, also known as the path metric unit (PMU) calculate new path metric values. in trellis each state can reached from the previous stage (from two states) so each current state have two path metric .The ACS unit adds current metric to every two branch coming to current state . Path metric unit then chose the least metric, and store it as the new path metric to current state.

3.3 Trace Back Unit (TBU)

After storing all possible survivor paths by ACSU, starting the decoding for a block of data (determined by the trace back length) through TBU.

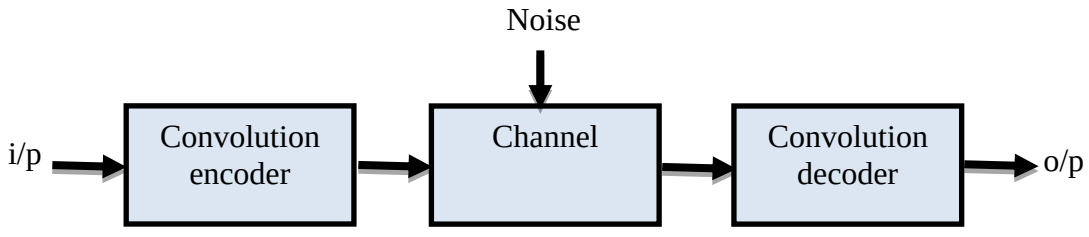
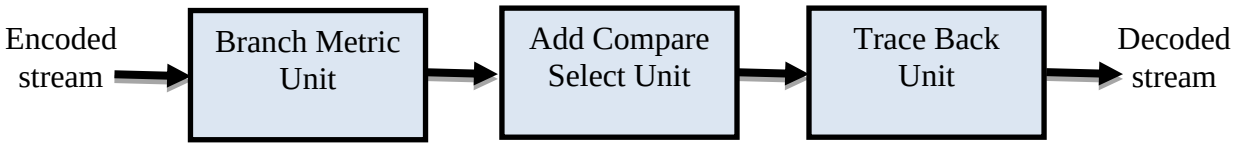


Fig. 2. Convolution Decoder



This is done by traces back the trellis .TBU starting from the path of the last survivor, for node of the minimum path and then trace back paths that return the path of the initial survivor track of state 0, then the original information data corresponding to the encoded data is determined.

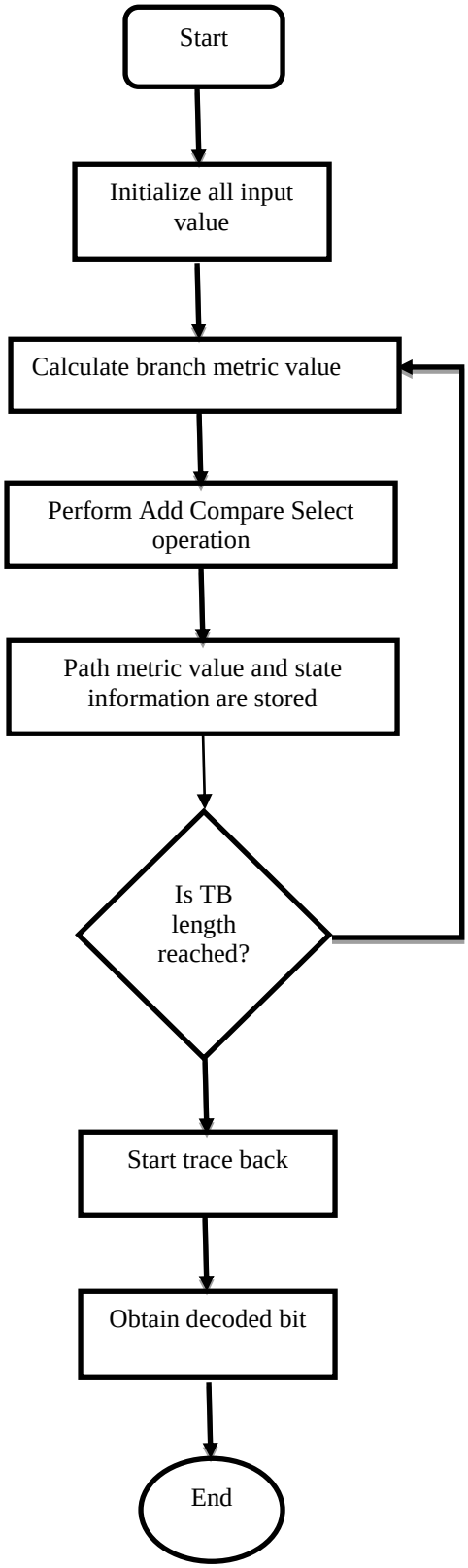


Fig. 4. Viterbi Decoder Flowchart

4. SIMULATION RESULT

In this paper, we generate (100000) random stream of binary bits, Signal to Noise Ratio (SNR) values are set from 0 to 10. A BPSK modulation is applied and signals are pass through AWGN channel, then, decoded by Viterbi decoder. Analyses performance of Viterbi decoder is perform by plotting the Bit Error Ratio (BER) versus (SNR) for AWGN channel. Simulation runs for different generator polynomials, and constraint lengths, also we take a varying trace back length. The constraint length equal (3,4,5, 6, and 7) with tracback length (10, 15, 20, 25, and 30). Fig. 5 shows a comparative between them in Bit Error Rate (BER) for hard decision decoder, while fig. 6 shows the BER for soft decision decoder. Fig. 7 compares between soft and hard decoder with different constraint length (6, and 7). Decoding time for soft and hard decoder with different constraint length is shown in fig. 8.

The theoretical BER is computed through equation 1

BER theo = 0.5*erfc (sqrt (SNR)) (1)

and trackback length calculated by equation 2:

(2 to 3) *(K-1) /(1-r) (2)

K=Constraint length

r=n/m. Refer to code rate.

To illustrate how to calculate traceback length, when K=3 and r=1/2, the result between (8 to 12).

5. CONCLUSIONS

The results shown in the above figures are simulate by Matlab2013a. Figures show that the performance of the Viterbi decoder in both hard and soft decoder in BER for different constraint lengths and polynomial equations with code rate=1/2. Soft decoder compare with hard decoder was shown to provide around (1 to 2) dB of gain for bit error rate, which can be noticed from figures (5 and 6). Further improvement in BER can be achieved by increasing the constraint length in both cases. At constraint lengths of 6 and 7, the designed Viterbi decoder had the highest performance calculated using BER and decoding time. The result show that the decoding time was faster in soft decision than in hard decision.

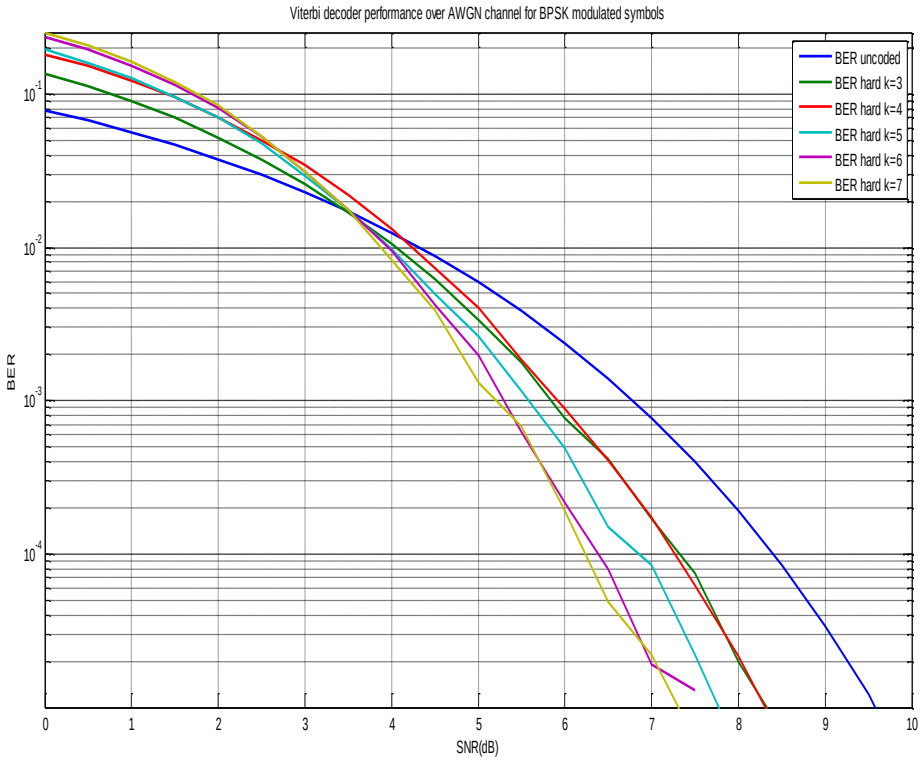


Fig. 6. Evaluating the performance of Soft Viterbi decoder by measuring BER at Different Constraint Lengths over AWGN channel for BPSK modulated symbols

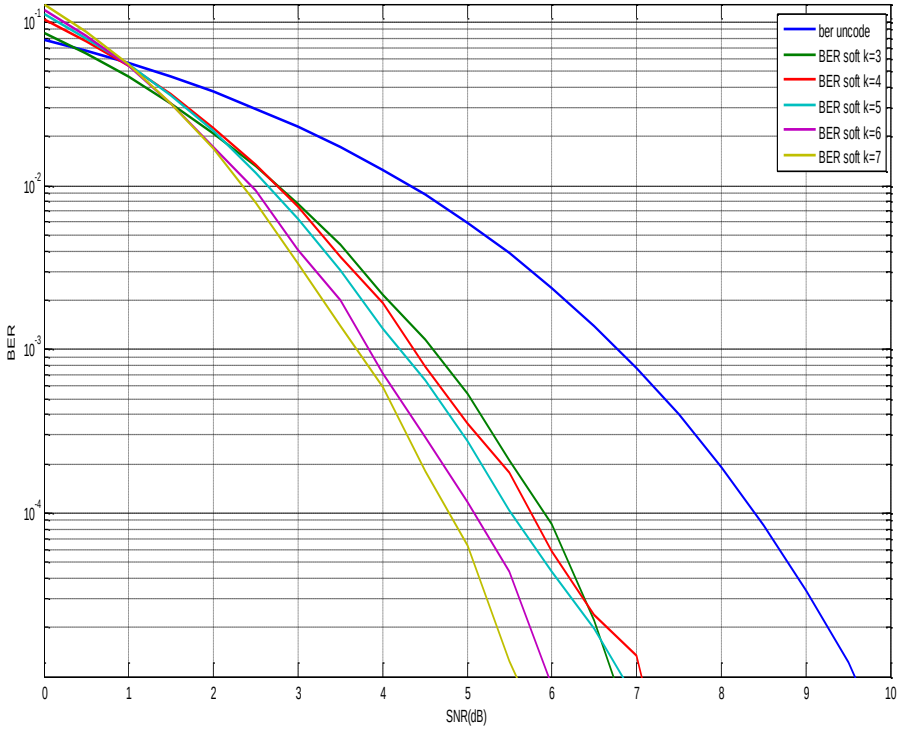


Fig. 5. Evaluating the performance of Hard Viterbi decoder by measuring BER at Different Constraint Lengths over AWGN channel for BPSK modulated symbols

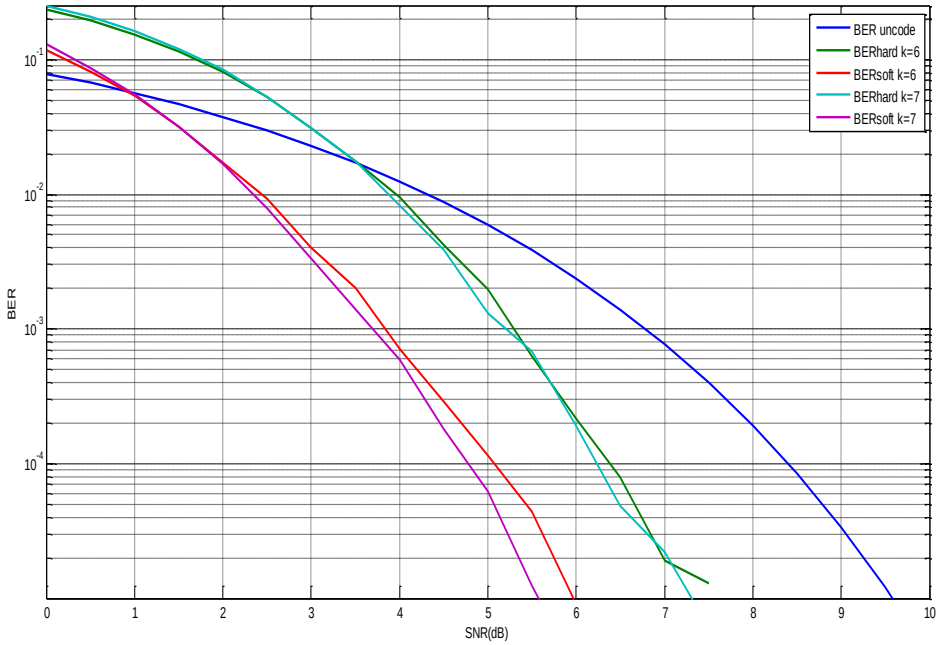


Fig. 7. Evaluating the performance of Soft and hard Viterbi decoder by measuring BER at Constraint Lengths of (6 and 7) over AWGN channel for BPSK modulated symbols

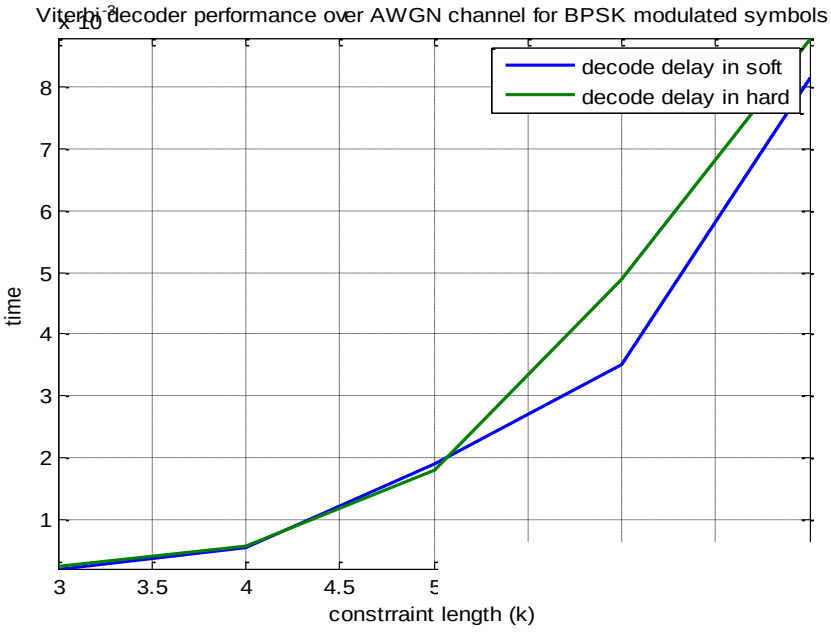


Fig. 8. Decoding delay for constraint length (3,4,5,6 and 7) in hard decoder and soft decoder

REFERENCES

[1] Minimization of Reversible Circuits for a Data Acquisition and Storage System, IJET, 2012, Vol. 2
[2] Jyoti, M. R. Tripathy and Vijeta, Comparison of Conditional Internal Activity Techniques for Low Power Consumption and High Performance Flip-Flops, International Journal of Computer Science and Telecommunications, ISSN 2047-3338, 2012, Vol. 3, Issue 2
[3] T. Kavitha and V. Sumalatha, A new Reduced Clock Power Flip Flop for future System On-Chip (SOC) Applications, IJCTT, 2012, Vol. 3.
[4] C. Kim and K. Roy, Dynamic Vt SRAM: a leakage tolerant cache memory for low voltage microprocessor, in Proc. of International Symposium on Low Power Electronics and Design, pp. 251-254, 2002.
[5] C. Kim, Memory World in the Next Decade, Memory Division, Device Solution Network Business, Samsung, Seminar presentation to Po-hang University of Science and Technology (POSTECH), Kyungpook, Korea, 2003.
[6] A. Lawrence, Processor Speed versus Memory, www.bleepingcomputer.com › Computer Tutorials › Hardware Tutorials, 2012.
[7] K. Mehta, N. Arora and B. P. Singh, Low Power Efficient D Flip Flop Circuit, International Symposium on Devices MEMS, Intelligent Systems & communication (ISDMISC, Proceedings published by International Journal of Computer Applications (IJCA), 2011.
[8] P. K. Meher, Extended Sequential logic for synchronous Circuit Optimization and its applications, TCADICS, 2008, IEEE (Pubs- permissions@ieee.org
[9] J. M. Ranjan, Tripathy and Vijeta, Comparison of Conditional Internal Activity Techniques for Low Power Consumption and High Performance Flip-Flops,JCST, , 2012, Vol. 3, Issue 2
[10] K. G. Sharma, T. Sharma, B. P. Singh & M. Sharma, Modified SET D-Flip Flop Design for Low-Power VLSI Applications, 2011.
[11] W. Stallings, Computer Organization and Architecture Designing for performance, Eighth Edition, Pearson Prentice Hall publication, 2010,
[12] D. T. Wang, Modern DRAM Memory Systems: Performance Analysis and Scheduling Algorithm, PhD dissertation, University of Maryland, U.S.A, 2005.